

FIG. 1

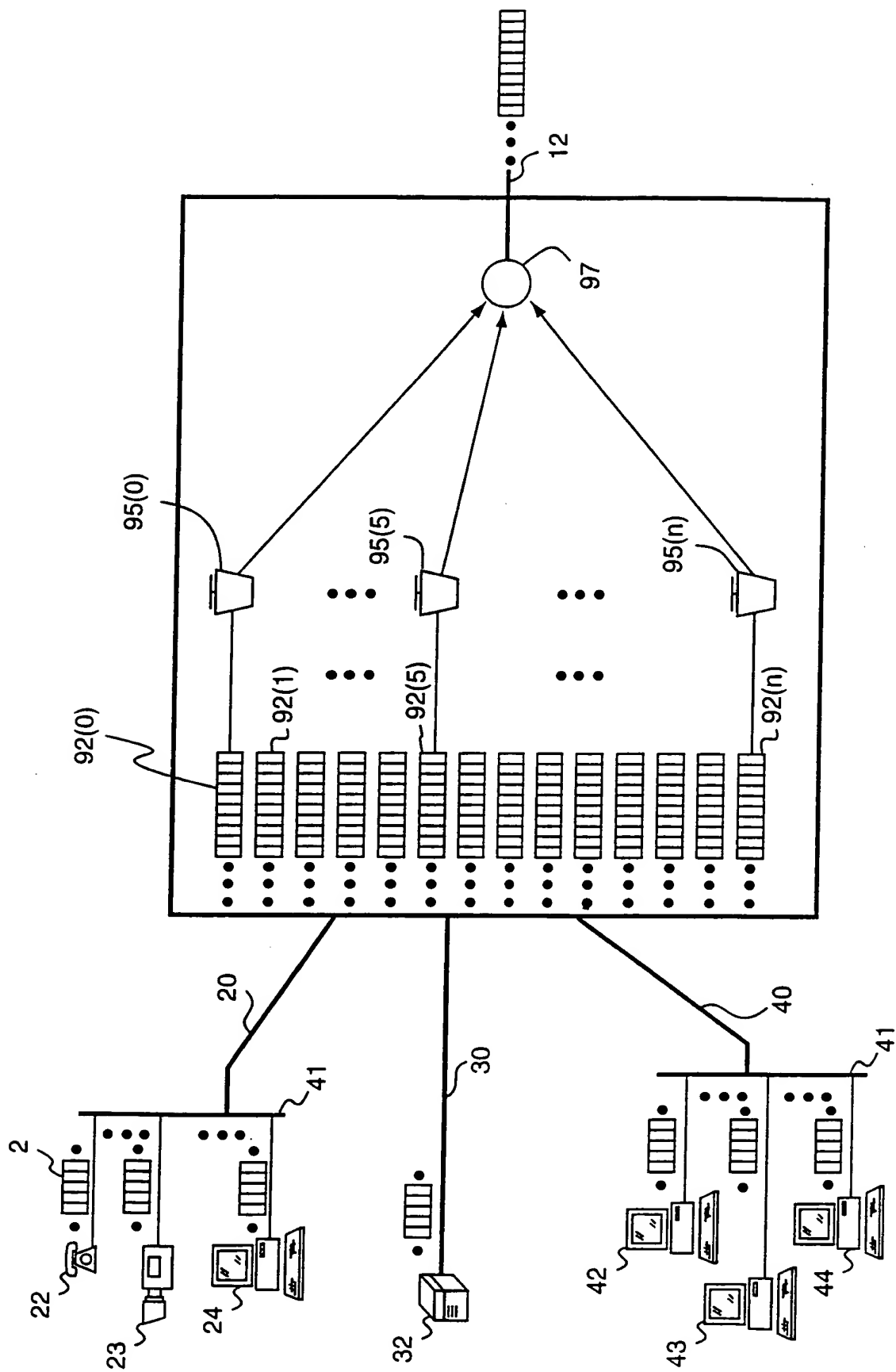


FIG. 2

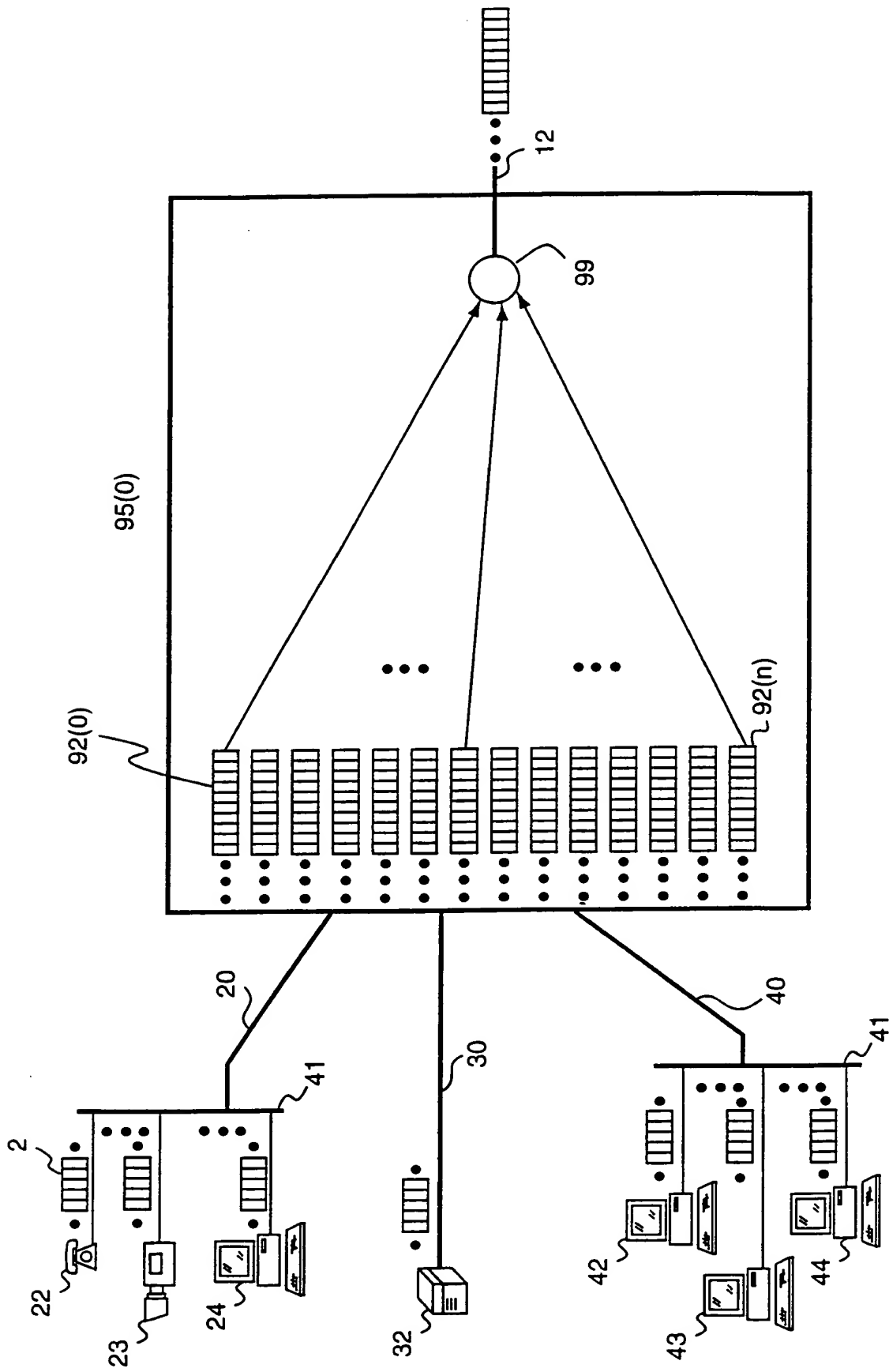


FIG. 3a

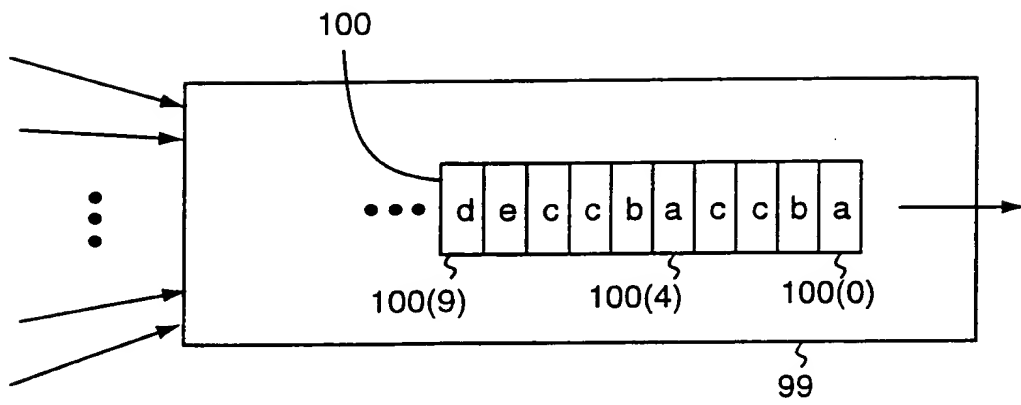


Fig. 3b

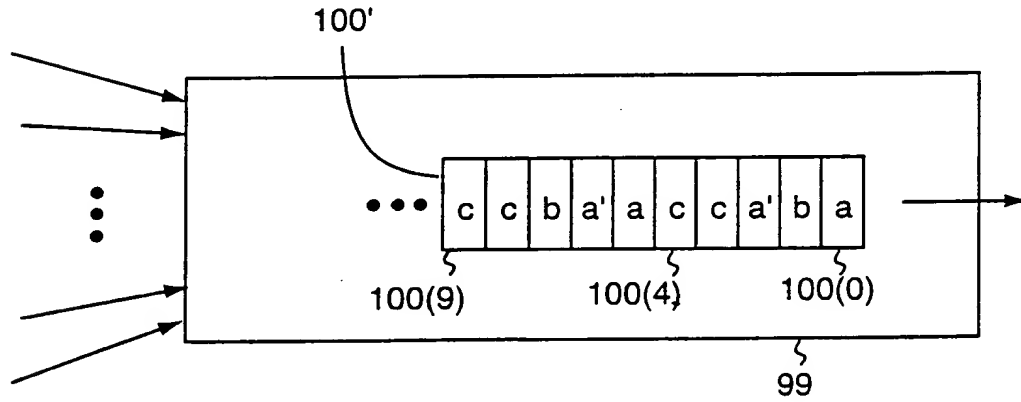


Fig. 3c

FIG. 4 is a block diagram of a parallel processing system 105. The system 105 includes a plurality of processing units 192(0) through 192(k). Each processing unit 192(i) includes a set of input registers 192(i,0) through 192(i,4), an adder 192(i,5), an AND gate 192(i,6), and a multiplexer 192(i,7). The input registers 192(i,0) through 192(i,4) are connected to the adder 192(i,5). The adder 192(i,5) is connected to the AND gate 192(i,6). The AND gate 192(i,6) is connected to the multiplexer 192(i,7). The multiplexer 192(i,7) is connected to a common bus 195. The common bus 195 is connected to a plurality of multiplexers 205(0) through 205(o). Each multiplexer 205(i) is connected to a register 200(i). The registers 200(0) through 200(o) are connected to a plurality of adders 202(0) through 202(o). Each adder 202(i) is connected to an AND gate 204(i). The AND gates 204(0) through 204(o) are connected to a common bus 207(p). The common bus 207(p) is connected to a processor 210. The processor 210 is connected to a memory 220.

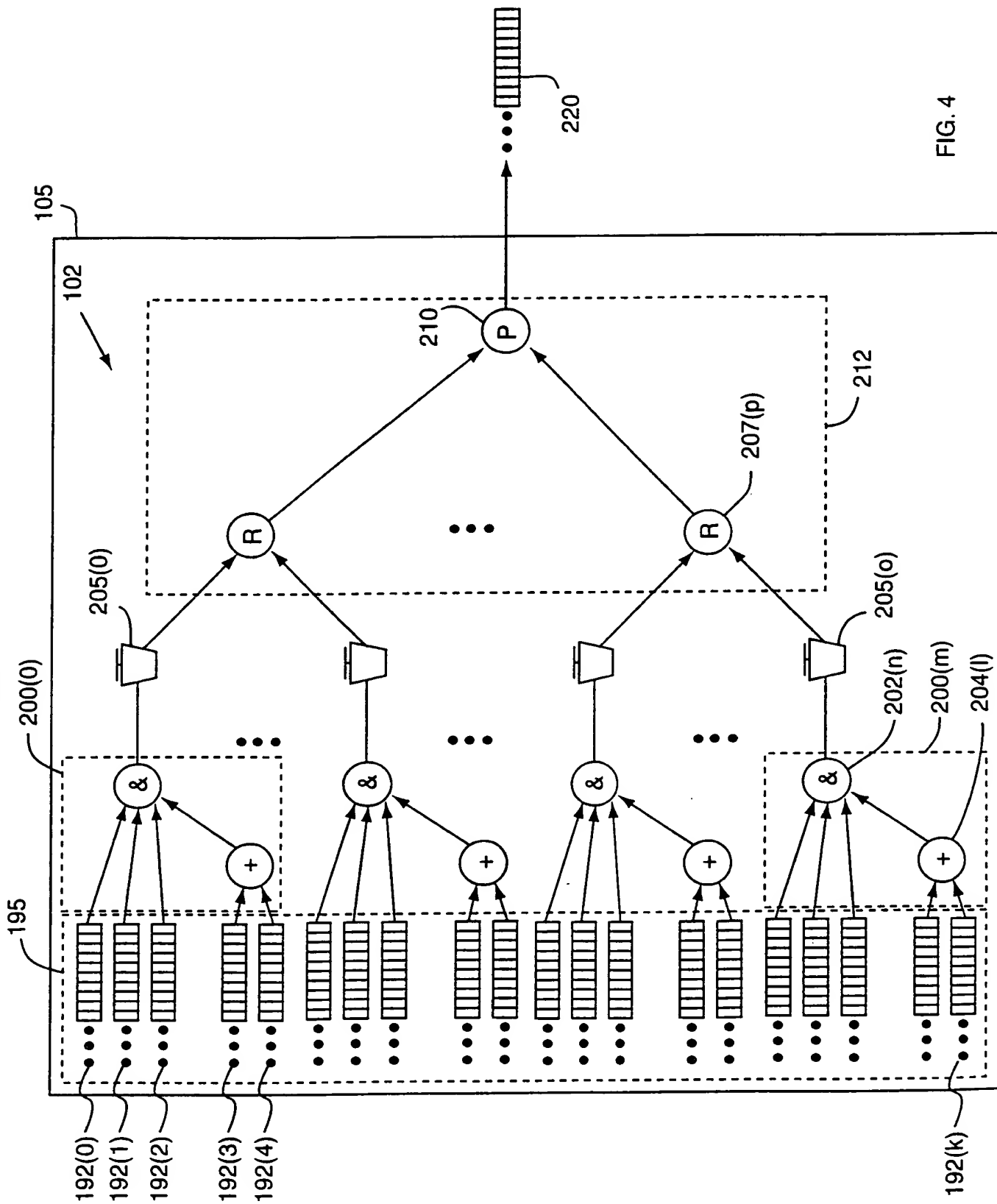


FIG. 4

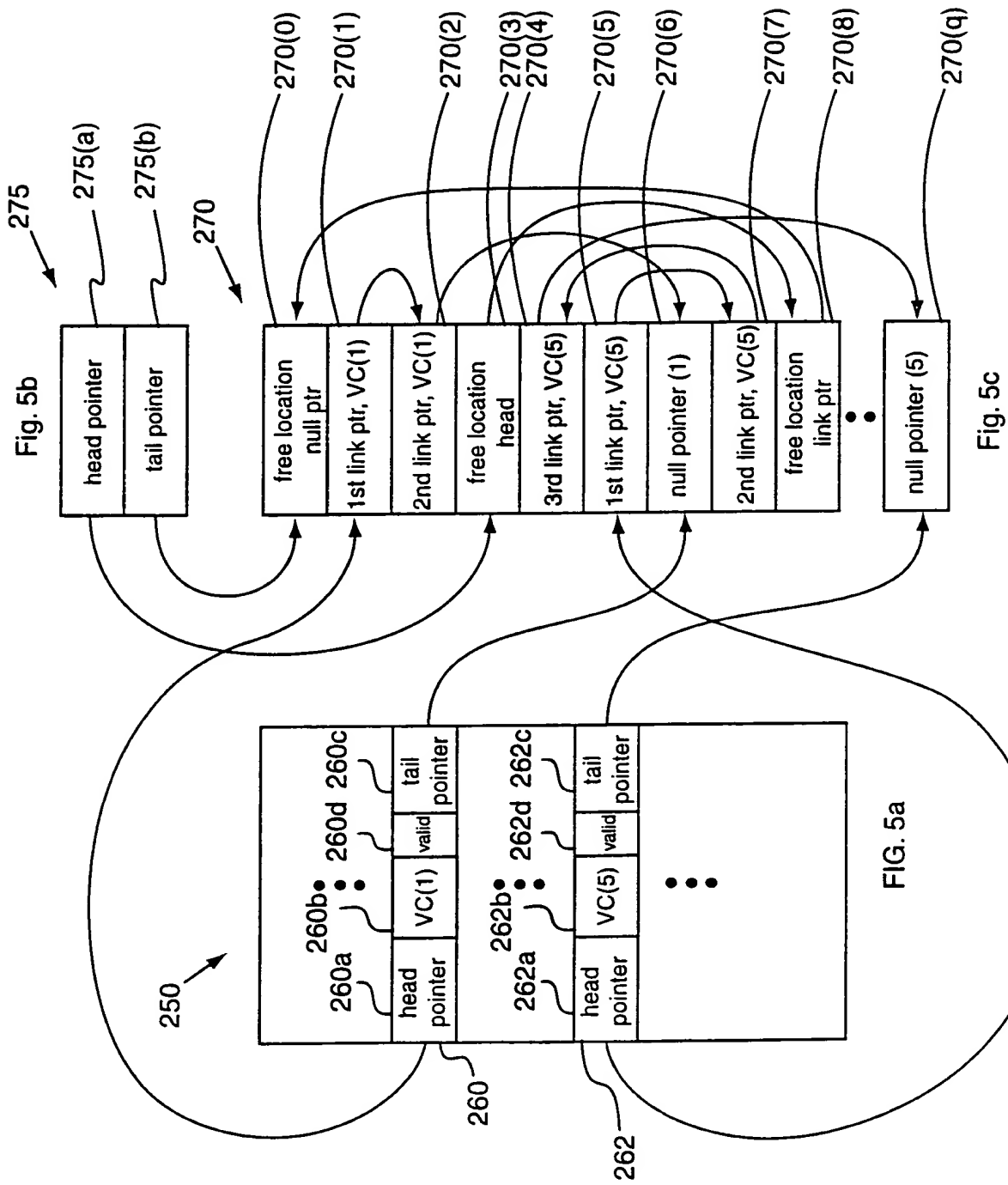


FIG. 5a

Fig. 5c

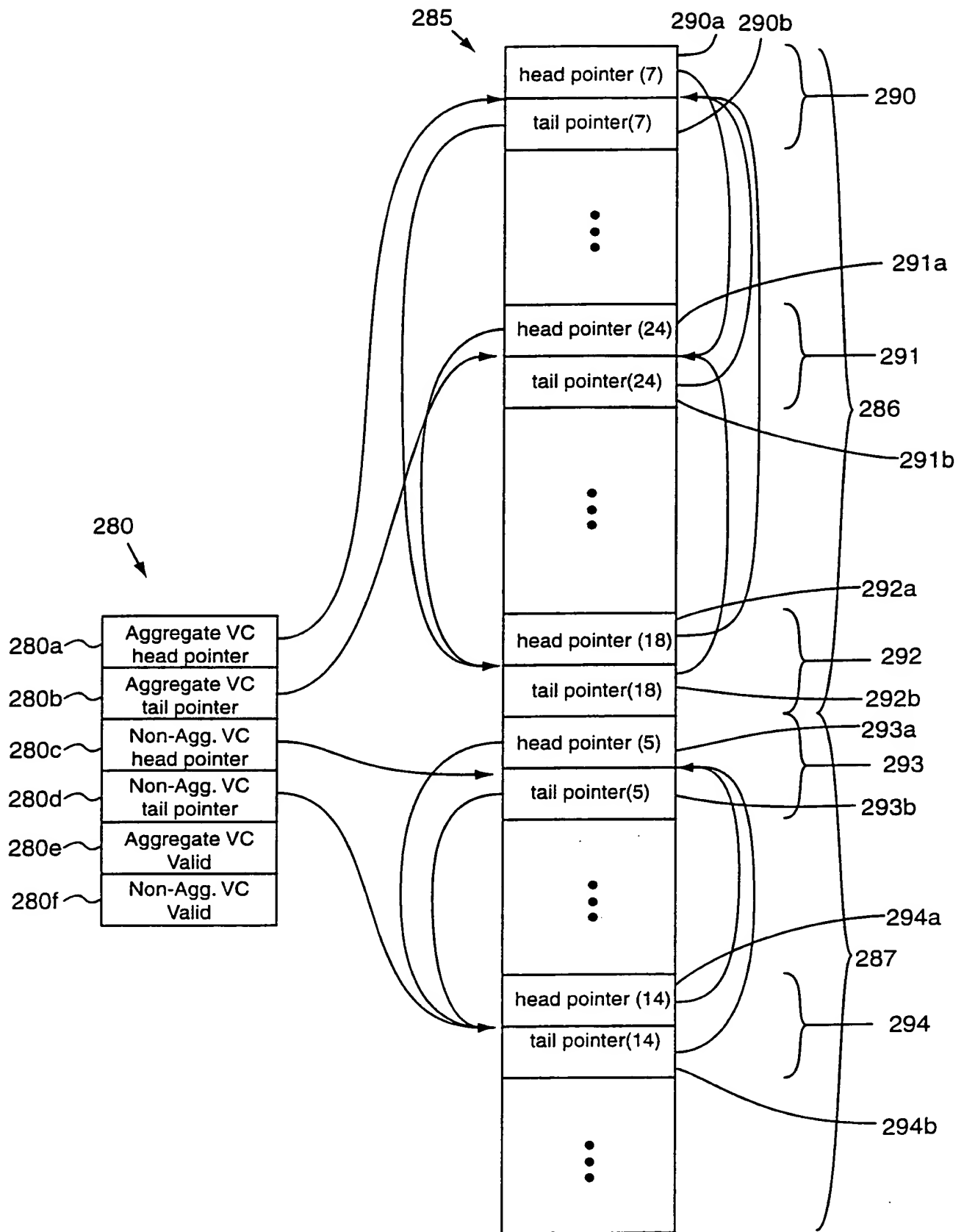


FIG. 6

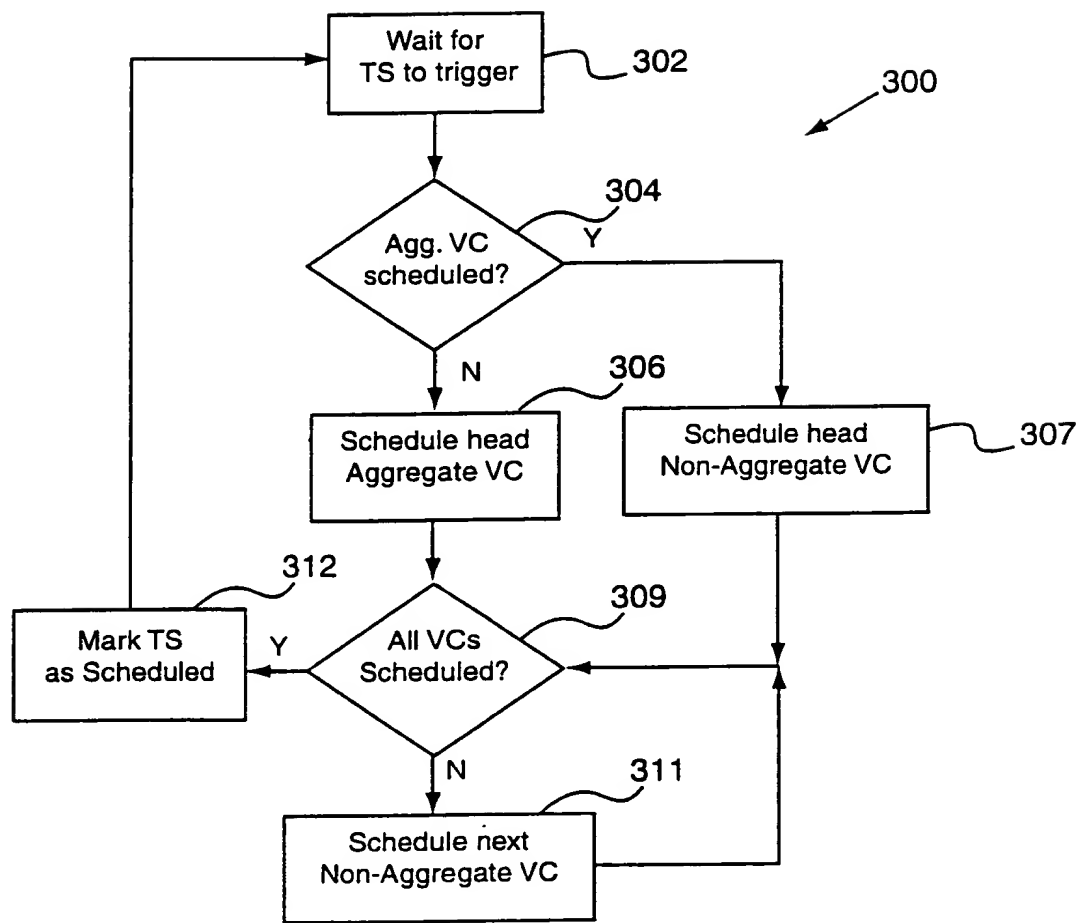


FIG. 7



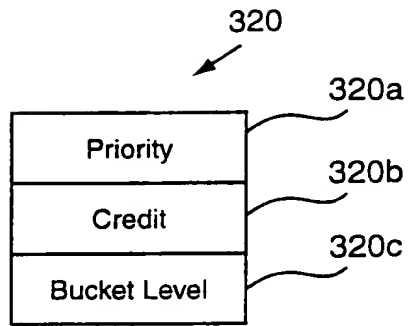


FIG. 8a

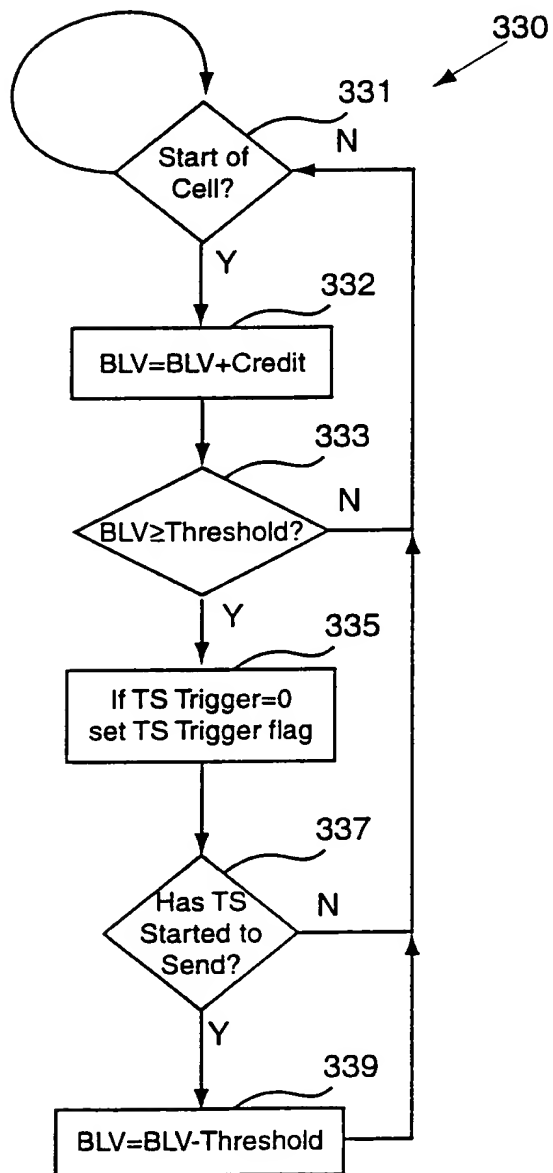


FIG. 8b

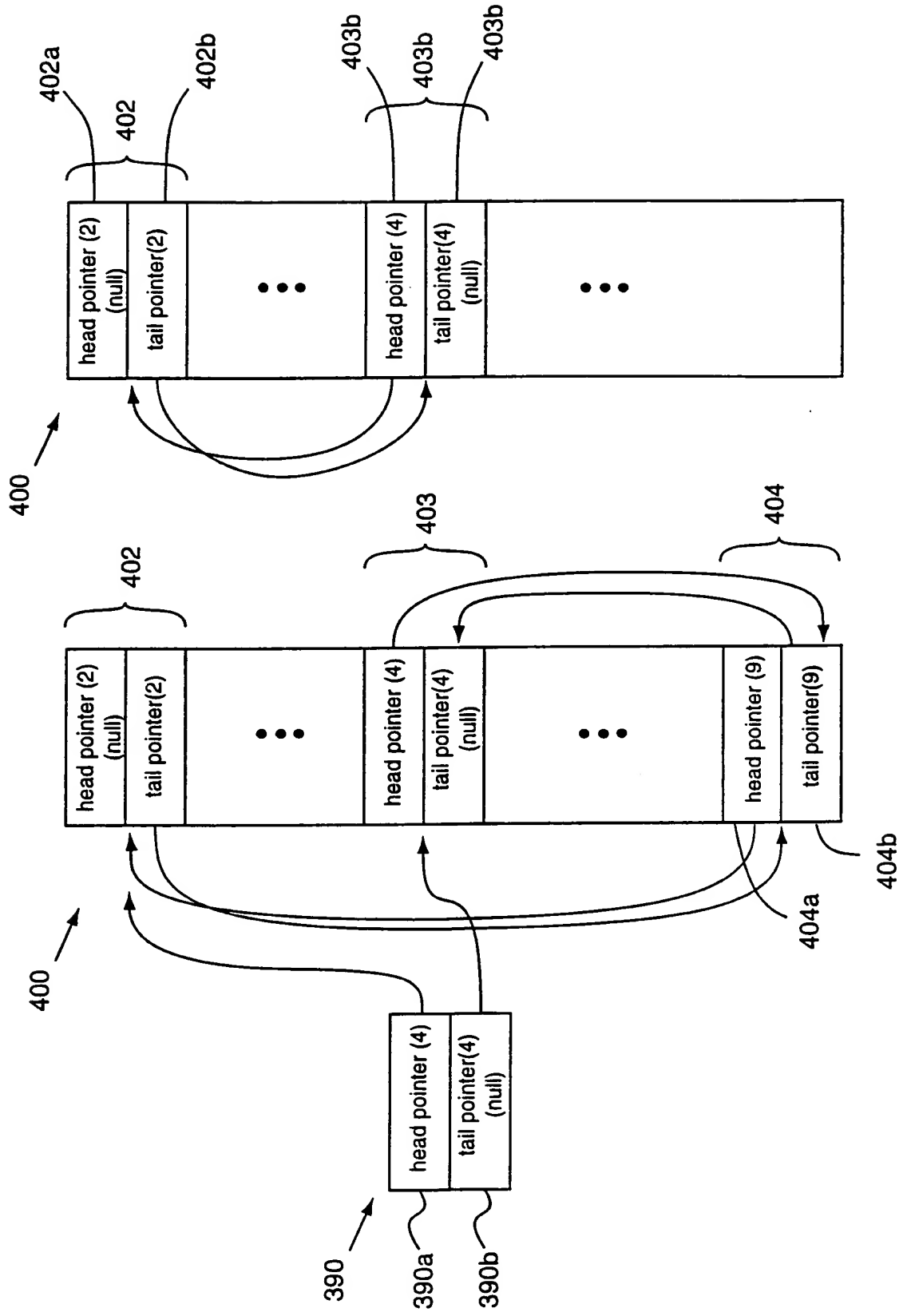


FIG. 9a

FIG. 9b

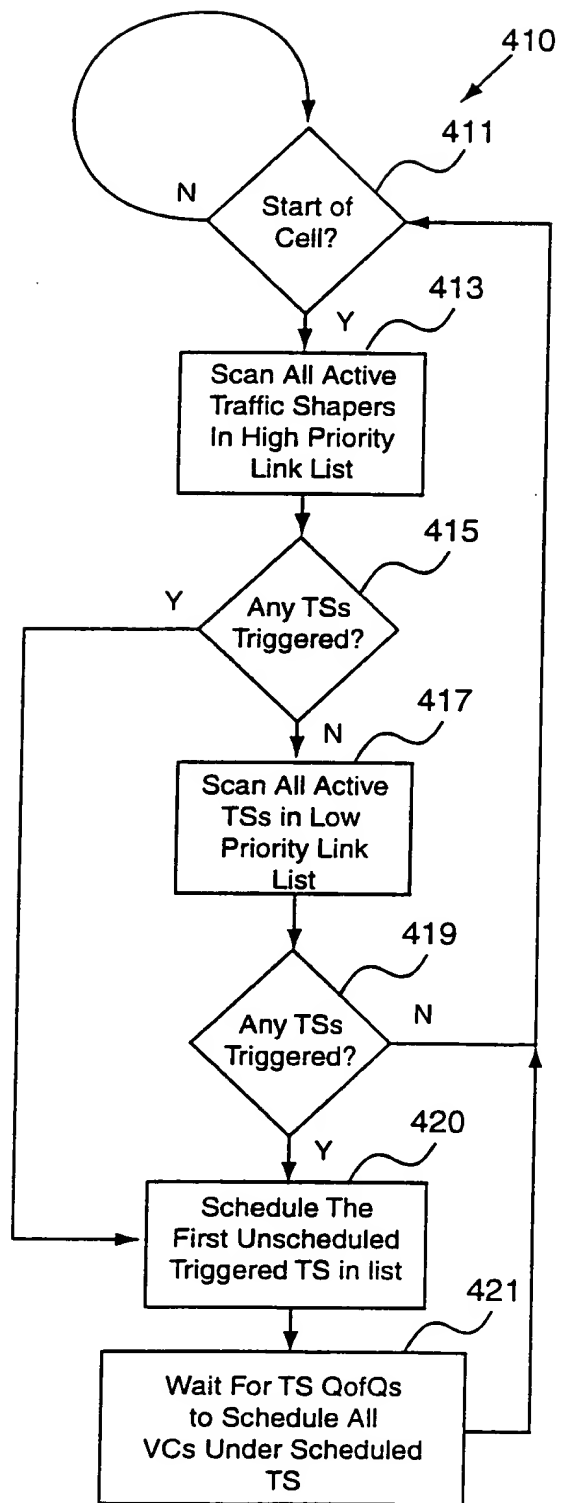


FIG. 10